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(54) **Display apparatus.**

(57) A display apparatus includes a matrix of a group of scanning lines and a group of data signal lines intersecting the scanning lines, pixels each formed at an intersection of the scanning lines and data signal lines, and a driver for supplying drive signals to the matrix so as to effect a display at the pixels. The scanning lines are divided into at least three blocks each comprising a plurality of adjacent scanning lines. The driver includes scanning means for sequentially selecting the at least three blocks so as not to select neighboring blocks consecutively and for consecutively selecting adjacent scanning lines in a selected block. As a result, flicker in a repetitive image is prevented while maintaining good observability of a motion picture.

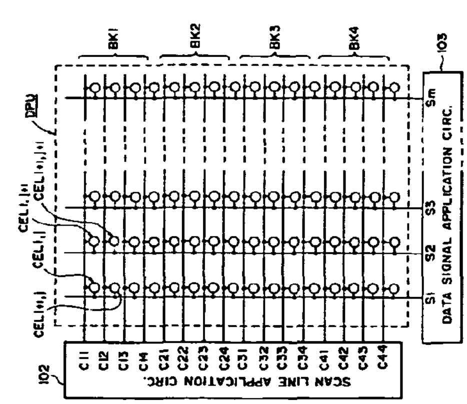

FIG. 1

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FIELD OF THE INVENTION AND RELATED ART

The present invention relates to a display apparatus for use in a television receiver, a computer terminal, an image data processing apparatus, such as a video camera view finder, etc., particularly a planar or flat panel-type display apparatus having scanning lines and data (signal) lines.

Planar display apparatus include, for example, a type using electron-discharging elements at respective pixels and a type using a liquid crystal for constituting pixels. Among others, a liquid crystal display apparatus using a liquid crystal has been widely used and is calling a further attention.

Hereinbelow, a display apparatus using a liquid crystal device, for example, will be described for convenience of comprehension.

There is a well-known type of liquid crystal display apparatus wherein a liquid crystal material is disposed between scanning lines (scanning electrodes) and data lines (data electrodes) constituting an electrode matrix so as to form a large number of pixels for displaying image data. The display apparatus is driven in a multiplexed manner such that an address or scanning signal is sequentially applied to the scanning electrodes, and prescribed data signals are applied in parallel to the data electrodes in synchronism with the address signal.

The sequential application of the address signal is performed according to various schemes, inclusive of the non-interlaced scanning scheme wherein the address signal is applied for selection to the scanning electrodes sequentially without skipping from one side to the other of the scanning electrodes, the two-interlaced scanning scheme wherein an address signal is sequentially applied to every other scanning electrode, and the N-interlaced scanning scheme (N = 3, 4, 5, ...) wherein an address signal is sequentially applied with skipping of two or more scanning electrodes apart, i.e., every N-th scanning electrode, as disclosed by Mihara et al in European published Patent Specification EP-A 316774. Particularly, in a display apparatus requiring a substantial selection term for one scanning electrode, a 2^n-interlaced scanning scheme of selecting every 2^n-th scanning electrode (n = 1, 2, 3, ...) is frequently used in order to suppress flicker due to scanning drive at a low-field frequency and in view of convenience of the scanning system.

Voltage change with time (i.e., voltage waveform) applied between electrodes (i.e. to a pixel) is different depending on whether the data signal applied thereto is for writing "black" or "white", so that the optical response of the pixel is different. More specifically, when the pixel concerned is on a selected scanning electrode, the pixel is switched to a black or white state. However, when the pixel concerned is on a non-selected scanning electrode, the pixel causes a change in luminance level depending on the data signal waveform while retaining the black or white. When a certain data electrode is alternately supplied with a black signal and a white signal, the pixels on the data electrode cause a change in luminance level in a cycle of alternation of the black and white signals throughout the period of non-selection of the pixels. If the alternation cycle is below a certain constant determined depending on the difference in luminance corresponding to the application of the black and white signals.

In a display apparatus, a repetitive image of each 2^n (n = an integer of 1, 2, 3, ...) is frequently used for convenience of a graphic system. In this instance, if the drive is performed according to the above-mentioned 2^n-interlaced scheme, flicker can occur due to periodical repetition of the white signal n some cases.

Further, if a higher degree of interlacing is adopted for increasing the field frequency so as to suppress flicker, the observability of a moving image (motion picture) can be lowered in some cases.

There is described a display apparatus adopting a driving scheme of sequentially selecting the scanning electrodes with skipping of a prescribed number of scanning electrodes apart so as to suppress the occurrence of flicker and improve the observability of a motion picture in U.S. Patent No. 5,172,105 entitled "DISPLAY APPARATUS" and issued to Katakura, et al.

On the other hand, there is a case where the scanning electrodes have to be sequentially selected one by one without skipping so as to display a complicated image in a good image quality or prevent the deterioration in image quality accompanying a temperature change. In such a case, it is difficult to apply the driving scheme disclosed by the above U.S. Patent as it is.

SUMMARY OF THE INVENTION

In view of the above problems, an object of the present invention is to provide a display apparatus capable of adopting a display drive scheme which suppresses the occurrence of flicker, improves the observability of a motion picture and is rich in wide applicability so that adjacent scanning lines are sequentially selected.

According to the present invention, there is provided a display apparatus, comprising: a matrix of a group of scanning lines and a group of data signal lines intersecting the scanning lines, pixels each formed at an intersection of the scanning lines and data signal lines, and drive means for supplying drive signals to the matrix so as to effect a display at the pixels;

the scanning lines being divided into at least three blocks each comprising a plurality of adjacent scanning lines,

the drive means including scanning means for sequentially selecting said at least three blocks so as not to select neighboring blocks consecutively and for consecutively selecting adjacent scanning lines in a selected block.

As described above, in the driving scheme adopted in the present invention, a selection signal is not applied to the scanning lines with skipping of a prescribed number of scanning lines from the beginning to the end of one vertical scanning as in the known drive scheme, but the blocks are selected with a spacing of at least one block, i.e., in a manner which may be called a "black-interlaced scanning" scheme. As a result, even in the case of displaying a repetitive image where "white" and "black" are alternately applied in a data line direction, the black data signal and white data signal continually alternate until the finish of line-sequential scanning within one block, so that the lowering in frequency of alternation of the black and white data signal is suppressed, thereby preventing the occurrence of flicker. Furthermore, non-interlaced scanning is performed within each block so that the observability of motion picture is maintained.

These and other objects, features and advantages of the present invention will become more apparent upon a consideration of the following description of the preferred embodiments of the present invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram for illustrating a basic structure of an embodiment of the display apparatus according to the invention.

Figure 2 is a time chart showing a set of scanning signals used in the display apparatus of Figure 1.

Figure 3 is a block diagram of a display apparatus or system according to the present invention.

Figure 4 is a partial schematic plan view of a liquid crystal display unit (picture area) used in the present invention, and Figure 5 is a schematic sectional view thereof.

Figures 6 and 10 are respectively a schematic view of blocks of scanning lines.

Figures 7, 9, 11, and 12 are respectively a conceptual view of memories used in the invention.

Figure 8 is a block diagram showing an algorithm used in the invention.

Figure 13 shows a set of drive signal waveforms used in the drive system of the present invention.

Figure 14 is a time chart showing time correlation between signal transfer and driving.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to a preferred embodiment of the present invention, there is provided a display apparatus having a plurality of scanning lines wherein a display screen or panel constituted by the scanning lines is divided into at least three regions (blocks) and the blocks are sequentially selected so that neighboring blocks are not consecutively selected, i.e., the blocks are selected with spacing of at least one block, and adjacent scanning lines within each block are consecutively selected in a non-interlaced scanning mode.

Herein, a basic structure of the display apparatus according to the present invention will be described with reference to Figure 1.

Figure 1 is a circuit diagram for illustrating a display apparatus. More specifically, Figure 1 shows a display unit DPU comprising a total of 14 scanning lines (C11 ... C14, C21 ... C24, ..., C41 ... C44) divided into four blocks (BK1, BK2, ..., BK4) each including four adjacent scanning lines.

CEL refers to a pixel and CELi,j generally refers to a pixel formed at the intersection of an i-th scanning line and a j-th data signal line. Each pixel provides a certain display data (optical data) based on a combination of two signals applied to the pixel, i.e., a signal supplied to an associated scanning line from a scanning signal application circuit 102 and a signal supplied to an associated one of data signal lines (S1 ... Sm).

In operation of the display apparatus thus constituted, as shown in a time chart of Figure 2, a block BK1 is selected first, and scanning lines C11 - C14 are sequentially scanned. Then, instead of a block BK2, a block BK3 is selected, and scanning lines C31 - C34 are sequentially scanned. Thereafter, the block BK2 is selected, and scanning lines C21 - C24 are sequentially scanned. Then, a block BK4 is selected, and scanning lines C41 - C44 are sequentially scanned. Thus, the blocks are scanned in a regularly or

irregularly interlaced manner, and the scanning lines in each block are scanned in a non-interlaced manner.

By repeating the above scanning scheme, a motion picture or a static picture is displayed on the display unit DPU.

For brevity of illustration, the scanning signal is depicted in a simple rectangular waveform in Figure 2. Actually, however, another appropriate waveform of scanning signal may also be used depending on the structure of the pixel, etc. Such a scanning signal can of course include a reset signal component (or clear signal component) for once resetting the display state of a pixel. The scanning signal can also include an auxiliary signal component for stabilizing the electrical or physical characteristic of a pixel without changing the display state of the pixel.

The timing of scanning signals applied to adjacent scanning lines in a block may be such that the falling of a preceding signal and the rising of a subsequent signal coincide each other or are spaced from each other with a prescribed interval. Alternatively, such successively applied two scanning signals can overlap each other. More specifically, in such a case, while a scanning line receives a signal component for display, a subsequent scanning line may receive a reset signal component so as to effect a high speed display.

The number of scanning lines selected at a time in each block need not be one, but a plurality of adjacent scanning lines can be selected simultaneously and such selection may be continued sequentially with respect to other pluralities of adjacent scanning lines.

As a more detailed description with reference to the arrangement shown in Figure 1, adjacent two scanning lines C11 and C12 are first selected, i.e., supplied with a scanning signal, simultaneously. Then, scanning lines C13 and C14 are selected simultaneously. Then, a subsequent block BK3 is selected with skipping of the block BK2, and C31 and C32 are selected simultaneously, followed by simultaneous selection of C33 and C34. Such operation is continued to effect one frame display.

In the case of simultaneous selection of a plurality of scanning lines as described above, it is also possible to effect a display such that two pixels CELi,j and CELi + 1,j on one data signal line constitute one combined pixel unit. In this case, one pixel, e.g., CELi,j, may be used as a standard pixel and another pixel CELi + 1,j may be used as a compensation pixel for effecting a display compensating for a possible difference in display state at the standard pixel from the time display state due to, e.g., a change in environmental temperature. Such a method is suitably adopted in gradational display performed by forming a transparent region and an opaque region in a pixel unit and by changing the ratio of the regions.

The pixels used in the present invention may suitably comprise a liquid crystal cell constituted, e.g., as a simple matrix display panel, an electro-luminescent cell including an electron-discharge device, or a liquid crystal cell having a switching element, such as a thin film transistor or an MIM element, at each pixel.

A liquid crystal cell is particularly preferred because of its economical production process, and suitable examples of the liquid crystal may include a twisted nematic liquid crystal and a ferroelectric liquid crystal as will be described hereinafter.

In case where the display unit (panel) is constituted as a transmission-type one, a light source as an illumination means may be disposed on one side thereof so as to improve the contrast and luminance.

It is further possible to dispose a recording means for recording a display image. Recording may be effected on recording media, such as magnetic media, optical media, semi-conductor memories, paper and plastic sheets, and recording means therefor may include a magnetic head, an optical head, a thermal head, and an ink jet head, for example.

The display apparatus according to the present invention may suitably be applied to a display method using a ferroelectric liquid crystal excellent in responsive characteristic and providing a wide viewing angle, particularly a gradational (gray-scale) display method using a ferroelectric liquid crystal (hereinafter sometimes abbreviated as "FLC").

Gradational display methods using FLC have been disclosed in, e.g., U.S. Patent No. 4,712,877 issued to Okada, et al; U.S. Patent No. 4,747,671 issued to Takahashi, et al, and U.S. Patent No. 4,763,994 issued to Kaneko et al.

More specifically, such gradational display methods may be representatively classified into (1) a method of dividing a pixel into sub-pixels which are controlled independently (dither method), (2) a method of forming a potential gradient in a pixel to divide the pixel into display regions (potential gradient method), (3) a method of applying a unidirectional electric field to a liquid crystal in a monostable state to control the deviation of the liquid crystal molecular long axis depending on the intensity of the electric field, and (4) a method of changing the liquid crystal layer thickness within a pixel to change the electric field intensity applied to the liquid crystal layer within the pixel, thus effecting a gradational display.

A problem in such a gradational display system using an FLC is that it causes a substantial change in threshold value corresponding to a temperature change, so that it is difficult to maintain an identical

gradation level in resistance to a temperature change. In order to solve the problem, we have proposed a driving scheme which may be called a pixel shift method (two pulse method) in U.S. Patent Application Serial No. 984,694, filed December 2, 1992 entitled "Liquid Crystal Display Apparatus". As an outline, the driving scheme includes: (1) writing line-sequentially from a first line to an n-th line, while (2) simultaneously selecting consecutive two scanning lines (L-th and L-th+1) at a selection time and, at a subsequent selection time, selecting simultaneously consecutive two scanning lines (L-th+1 and L-th+2) deviated by one line, wherein L is an integer satisfying $1 \leq L \leq n$. Of the consecutive L-th and L-th+1 scanning lines, the L-th scanning line is a scanning line for temperature compensation for the L-th+1 scanning line. More specifically, if the liquid crystal cell is at a standard temperature, only the L-th+1 scanning line is written and, if the temperature deviates, the L-th line is written. In other words, display data to be displayed on the L-th+1 scanning line is shifted onto the L-th scanning line in accordance with a temperature change. Thus, an undesirable display state of a pixel on one scanning line of adjacent at least two scanning lines is compensated by a display state of a pixel on the other scanning line. That is, a synthetic display state of adjacent pixels on a data line and at least two scanning lines is used as a unit of gradational display. By this measure, an undesirable display state of a pixel in the unit can be compensated by a display state of the remaining pixel in the unit, whereby a normal display can be achieved as a whole.

In order to realize the above-described writing operation, the following conditions may be set. (3) The simultaneously selected (at least) two scanning lines are supplied with mutually different scanning signals, which are determined to provide continuous thresholds at two pixels formed at the intersections of a data line and the two scanning lines. The provision of "continuous threshold" is a condition for realizing a smooth data shift between two scanning lines which are sequentially written by a line-sequential scan. (4) A pixel is required to have a distribution of thresholds with respect to transmittance.

In such a driving method, however, image data changes its position according to a temperature change, so that it is difficult to completely display a one frame picture. More specifically, the pixels on the first scanning line are not provided with a scanning line to which image data is shifted, and the pixels on the n-th scanning line are not subjected to an operation after the image data shift according to a temperature change.

Secondly, as the scanning lines are selected line-sequentially from the first line to the n-th line, interlaced scanning cannot be performed.

The present invention may be suitably applied to suppressing the flickering liable to be caused in the above-mentioned gradational drive scheme.

Hereinbelow, the present invention is described more specifically based on preferred embodiments.

[First embodiment]

Figure 3 is a block diagram showing a liquid crystal display apparatus according a first embodiment of the present invention. Referring to Figure 3, the display apparatus includes a liquid crystal display unit (panel) 101, a scanning signal application circuit 102, a data signal application circuit 103, a scanning signal control circuit 104, a drive control circuit 105, a data signal control circuit 106 and a graphic controller 107.

Data supplied from the graphic controller 107 through the drive control circuit 105 enter the scanning signal control circuit 104 and the data signal control circuit 106 where they are converted into address data and display data, respectively. According to the address data, the scanning signal application circuit 102 generates scanning signals which are supplied to the scanning electrodes in the liquid crystal display unit 101. Further, according to the display data, the data signal application circuit 103 generates data signals, which are supplied to the data electrodes in the liquid crystal display unit 101.

Figure 4 is an enlarged partial view of the liquid crystal display unit 101 which includes scanning electrodes C1 - C6 ... and data electrodes S1 - S6 ... disposed so as to form an electrode matrix and form pixels each constituting a display unit, including, e.g., a pixel P22 formed at the intersection of a scanning electrode C2 and a data electrode S2. Figure 5 is a partial sectional view of the display unit taken along the line A - A in Figure 4. Referring to Figure 5, the liquid crystal display unit 101 includes glass substrates 302 and 304 and a ferroelectric liquid crystal 303 disposed between the substrates 302 and 304 and in a cell structure forming a cell gap defined by a spacer 306. Further, an analyzer 301 and a polarizer 305 are disposed in cross nicols so as to sandwich the cell structure.

More specifically, the cell structure shown in Figures 4 and 5 comprises a pair of substrates 302 and 304 made of glass plates or plastic plates which are held with a predetermined gap with spacers 306 and sealed with an adhesive to form a cell structure filled with a liquid crystal. On the substrate 304 is further formed an electrode group (e.g., an electrode group for applying scanning voltages of a matrix electrode structure) comprising a plurality of transparent electrodes C1 - C6 ... in a predetermined pattern, e.g., of a

stripe pattern. On the substrate 302 is formed another electrode group (e.g., an electrode group for applying data voltages of the matrix electrode structure) comprising a plurality of transparent electrodes S1 - S6 ... intersecting with the transparent electrodes C1 - C6.

In the device, the alignment control films (not shown) may be directly disposed over the transparent electrodes C1 - C6 and S1 - S6 formed on the substrates 304 and 302, respectively. In another embodiment, on the substrates 304 and 302, insulating films for short circuit prevention (not shown) and alignment control films (not shown) may be disposed, respectively.

Examples of the material constituting the alignment control films may include inorganic insulating materials, such as silicon monoxide, silicon dioxide, aluminum oxide, zirconia, magnesium fluoride, cerium oxide, cerium fluoride, silicon nitride, silicon carbide, and boron nitride; and organic insulating materials, such as polyvinyl alcohol, polyimide, polyamide-imide, polyester-imide, polyparaxylylene, polyester, polycarbonate, polyvinyl acetal, polyvinyl chloride, polyamide, polystyrene, cellulose resin, melamine resin, urea resin and acrylic resin. The above-mentioned alignment (control) film of an insulating material can be also used as an insulating film for short circuit prevention.

The alignment control films of an inorganic insulating material or an organic insulating material may be provided with a uniaxial alignment axis by rubbing the surface of the film after formation thereof in one direction with velvet, cloth or paper to form the uniaxial alignment axis.

Further, the insulating films for short circuit prevention may be formed in a thickness of 200 Å or larger, preferably 500 Å or larger, with an inorganic insulating material, such as SiO_2, TiO_2, Al_2O_3, Si_3N_4 and $BaTiO_3$. The film formation may for example be effected by sputtering, ion beam evaporation, or calcination of an organic titanium compound, an organic silane compound, or an organic aluminum compound. The organic titanium compound may for example be an alkyl (methyl, ethyl, propyl, butyl, etc.) titanate compound, and the organic silane compound may be an ordinary silane coupling agent. In case where the thickness of the insulating films for short circuit prevention is below 200 Å, a sufficient short circuit prevention effect cannot be accomplished. On the other hand, if the thickness is above 5000 Å, the effective voltage applied to the liquid crystal layer is decreased substantially, so that the thickness may be set to 5000 Å or less, preferably 2000 Å or less.

The liquid crystal material suitably used in the present invention is a chiral smectic liquid crystal showing ferroelectricity. More specifically, liquid crystals in chiral smectic C phase (SmC*), chiral smectic G phase (SmG*), chiral smectic F phase (SmF*), chiral smectic I phase (SmI*) or chiral smectic H phase (SmH*) may be used.

Details of ferroelectric liquid crystals may be disclosed in, e.g., LE JOURNAL DE PHYSIQUE LETTERS, 36 (L-69) 1975, "Ferroelectric Liquid Crystals"; Applied Physics Letters 36 11, 1980, "Submicro Second Bistable Electrooptic Switching in Liquid Crystals"; Kotai Butsuri (Solid-State Physics) 16 (141) 1981, "Ekisho (Liquid Crystals)"; U.S. Patents Nos. 4,561,726; 4,589,996; 4,592,858; 4,596,667; 4,613,209; 4,614,609; 4,622,165, etc. Chiral smectic liquid crystals disclosed in these references can be used in the present invention.

Other specific examples of ferroelectric liquid crystal may include decyloxybenzylidene-p'-amino-2-methylbutylcinnamate (DOBAMBC), hexyloxybenzylidene-p'-amino-2-chloropropylcinnamate (HOBACPC), and 4-O-(2-methyl)butylresorcylidene-4'-octylaniline (MBRA 8).

[First Embodiment]

As for the liquid crystal display apparatus embodiment shown in Figures 3 - 5, when the selecting term for one scanning electrode is 96 usec, the frame frequency becomes 1/(512 x 96 µsec) = 20.3 Hz. In this display apparatus, if the field frequency is 40 Hz or higher, flickering caused by scanning drive is suppressed, so that one picture is designed to be formed by two times of vertical scanning.

As shown in Figure 6, the whole picture area composed of 512 lines (scanning electrodes) is divided into 16 blocks B1 - B16. In a first field, blocks B1, B3, B5, B7, B9, B11, B13 and B15 are selected and, in a second field, blocks B2, B4, B6, B8, B10, B12, B14 and B16 are selected. In each block, non-interlaced scanning is performed. As an overall scanning sequence, 1st, 2nd, 3rd, ..., 31th, 32th, 65th, 66th ..., 96th, 129th, 130th, ..., 160th, ..., 449th, 450th, ... and 480th scanning electrodes are sequentially selected to complete first vertical scanning, and then 33th, 34th, 35th, ..., 63th, 64th, 97th, 98th, ..., 128th, 161th, 162th, ..., 192th, ..., 481th, 482th, ... and 512th scanning electrodes are sequentially selected to complete second vertical scanning, thus writing one whole picture.

For accomplishing the above method, a memory 500 as shown in Figure 7 is provided in the scanning signal control circuit 104. Referring to Figure 7, the memory 500 includes a scanning address memory M1, an address increment memory M2, a line-number counter memory M3, a block-number counter memory,

and address table memories MT(1) - MT(16). As fixed values, the number of 1 is set at the address increment memory M2, and the 16 numbers of 1, 65, 129, 193, 257, 321, 385, 449, 33, 97, 161, 225, 289, 353, 417 and 481 are set at the address table memories MT(1) - MT(16), respectively, as the starting scanning address (positional ranks of the starting scanning electrodes) among the entire scanning electrodes for the first vertical scanning and the second vertical scanning in that order. Here, the content of the scanning address memory means the scanning address. The content of the address increment memory M2 means the number of scanning electrodes covered by one-time of scanning (namely "1" means that every line is scanned in a non-interlaced manner). The content of the line-number counter memory means the number of times of scanning effected at that time in each block. The content of the block-number counter memory M4 means the ordinal number of block for which the scanning is performed at that time throughout the first vertical scanning and second vertical scanning. The contents of the address table memories MT(1) - MT(16) mean the scanning addresses from which the scanning is started for the respective blocks.

Figure 8 is a flow chart showing an algorithm for determining the scanning addresses. At Step 1, the number of "1" is set in the block-number counter memory M4 for initialization. At Step 2, the number in the block-number counter memory M4 is checked as to whether it exceeds 16 (M4 > 16) in order to judge whether all the blocks have been written. At Step 3, the line-number counter memory is initialized for scanning in each block. First of all, a number of "1" is set in the line-number counter memory M3 for first scanning in the block. Then, so as to determine the starting scanning address in the block concerned, the number of the block is checked according to the content of the block-number counter memory, and the starting scanning address in the block is checked according to the content of the corresponding address table memory MT to set the starting scanning address at the scanning address memory M1. At Step 4, a number "1" is added to the block-number counter memory M4. At Step 5, it is checked whether the content of the line-number counter memory M3 exceeds 32 (M3 > 32) so as to judge whether the writing in the block has been completed. At Step 6, the scanning address is transferred. At Step 7, the content of the address increment memory M2 is added to the content of the scanning address memory M1, and a number of "1" is added to the line-number counter memory M3.

Thus, according to the algorithm shown in Figure 8, the content of the address table memory MT is set to the scanning address memory M1 based on the content of the block-number counter memory M4, and this operation is repeated 16 times, during each of which the steps of sending the scanning address to the scanning signal application circuit and increasing the content of the scanning line address memory by "1" (the content of the address increment memory M2) are repeated 32 times. After the scanning address is transferred 16x32 times, the operation is restored to the beginning. Before the first transfer of scanning address, a number of "1" is set at each of the scanning address memory M1, the line-number counter memory M3 and the block-number counter memory M4.

Now, if an image as shown in Figure 4 is taken for example, wherein the pixels on the odd-numbered scanning electrodes, i.e., 1st, 3rd, 5th ... to 511th lines, are in black, and the pixels on the even-numbered scanning electrodes, i.e., 2nd, 4th, 6th ... to 512th lines alternately assume black, white, black, white, ..., a pixel P22 repetitively receives black signal and white signal for each one line. The frequency of repetition is $1/(1 \times 2 \times 96\ \mu\text{sec}) = 5208$ Hz (> 40 Hz), so that no flickering occurs.

On the other hand, if a similar image is displayed according to the conventional 2-interlaced scanning scheme, the 1st, 3rd, 5th ... to 511th lines are sequentially selected to complete the first vertical scanning, and subsequently the 2nd, 4th, ... to 512th lines are sequentially selected to complete the second vertical scanning, whereby one whole picture is written. In this case, the pixel P22 continuously receives the black signal 256 times and then continuously receives the white signal 256 times, so that the signal repetition frequency becomes $1/(256 \times 2 \times 96\ \mu\text{sec}) = 20.3$ Hz (< 40 Hz), whereby flickering is observed.

Further, if the 8-interlaced scanning scheme is adopted so as to obviate flickering, while the flickering is removed due to an increased frequency, the observability of a motion picture is remarkably impaired because a picture is constituted by scanning of every 8th line in comparison with the non-interlaced scanning.

[Second embodiment]

In order not to lower the field frequency below 40 Hz, it is also possible to select the blocks at random so as to write one whole picture. For example, the apparatus used in the first embodiment may be driven by selecting the blocks in the order of B1, B10, B3, B8, B13, B2, B15, B12, B5, B14, B7, B16, B9, B6, B11 and B4 to achieve a similar effect.

In this instance, 16 numbers of 1, 289, 65, 225, 385, 33, 449, 353, 129, 417, 193, 481, 257, 161, 321 and 97 are set at the address table memories MT(1) - MT(16), respectively, as shown in Figure 9.

[Third Embodiment]

In this embodiment, a liquid crystal display apparatus is constituted by 1024 scanning electrodes and 1280 data electrodes disposed to form an electrode matrix.

When the selecting term for one scanning electrode is 96 µsec, the frame frequency becomes 1/(1024 x 96 µsec) = 10.2 Hz. So as to provide a field frequency of 40 Hz or higher, a whole picture is designed to be formed by four times of vertical scanning.

As shown in Figure 10, the 1024 scanning lines constituting a whole display area are divided into 32 blocks B1 - B32 each including 32 lines. In a first field, blocks B1, B5, B9, B13, B17, B21, B25 and B29 are selected in this order. Further, blocks B3, B7, B11, B15, B19, B23, B27 and B31 are selected in a second field; blocks B2, B6, B10, B14, B18, B22, B26 and B30 are selected in a third field; and blocks B4, B8, B12, B16, B20, B24, B28 and B30 are selected in a fourth field. And, in each field, the scanning lines are subjected to non-interlaced scanning.

As an overall sequence, 1st, 2nd, 3rd, ..., 31th, 32th, 129th, 130th, ..., 160th, 257th, 258th, ..., 288th, ..., 897th, 898th, ..., and 928th scanning lines are selected to complete first vertical scanning; 65th, 66th, 67th, ..., 95th, 96th, 193th, 194th, ..., 224th, 321th, 322th, ..., 352th, 961th, 962th, ..., and 992th scanning lines are selected to complete second vertical scanning; 33th, 34th, 35th, ..., 63th, 64th, 161th, 162th, ..., 192th, 289th, 290th, ..., 320th, ..., 929th, 930th, ..., and 960th scanning lines are selected to complete third vertical scanning; and then 97th, 98th, 99th, ..., 127th, 128th, 225th, 226th, ..., 256th, 353th, 354th, ..., 384th, 993th, 994th, ..., and 1024th scanning lines are selected to complete fourth vertical scanning, thus writing one whole picture.

For accomplishing the above method, a memory 800 as shown in Figure 11 is provided in the scanning signal control circuit. As fixed values, a number of 1 is set at the address increment memory M2, and 32 numbers of 1, 129, 257, 385, 513, 641, 769, 897, 65, 193, 321, 449, 577, 705, 833, 961, 33, 161, 289, 417, 545, 673, 801, 929, 97, 225, 353, 481, 609, 737, 865 and 993 are set at the address table memories MT(1) - MT(32), respectively, as the starting scanning addresses among the entire scanning lines for the first, second, third and fourth vertical scanning.

The scanning address is performed according to the same algorithm as shown in Figure 8 except that the number of blocks for judging completion of writing in all the blocks is changed to M4 > 32 at step 2 in Figure 8.

If an image as shown in Figure 4 is taken for example, wherein the pixels on the odd-numbered scanning electrodes, i.e., 1st, 3rd, 5th, ... to 1023th lines are in black, and the pixels on the even-number scanning electrodes, i.e., 2nd, 4th, 6th, ..., 1024th lines, are in white, a pixel P22 receives a black signal and a white signal alternately for each one line. The frequency of repetition is 1/(1x2x96 µsec) = 5208 Hz (> 40 Hz).

On the other hand, if a similar image is displayed according to a known 4-interlaced scanning scheme, 1st, 5th, 9th, ..., and 1021th scanning lines are selected to complete 1st vertical scanning; 2nd, 6th, 10th, ... and 1022th scanning lines are selected to complete 2nd vertical scanning; 3rd, 7th, 11th, ... and 1023th scanning lines are selected to complete 3rd vertical scanning; and then 4th, 8th, 12th, ... and 1024th scanning lines are selected to complete 4th vertical scanning, thus writing one whole picture. In this case, the pixel P22 continuously receive the black signal 256 times, then the white signals 256 times, then the black signal 256 times and then the black signal 256 times, so that the repetition frequency becomes 1/-(256x2x96 µsec) = 20.3 Hz (< 40 Hz), whereby flicker is observed.

Further, if a 16-interlaced scanning scheme is adopted so as to obviate flicker, while the flicker is removed due to an increased frequency, the observability of a motion picture is remarkably impaired because a picture is constituted by scanning of every 16th line in comparison with the non-interlaced scanning.

[Fourth embodiment]

In order not to lower the field frequency below 40 Hz, it is also possible to select the blocks at random so as to write one whole picture. For example, the apparatus in the third embodiment may be driven by selecting the blocks in the order of B1, B18, B27, B12, B5, B22, B31, B8, B17, B2, B23, B20, B29, B14, B11, B32, B13, B26, B3, B16, B9, B30, B19, B4, B25, B10, B7, B28, B21, B6, B15 and B24 to achieve a similar effect. In this instance, 32 addresses of 1, 545, 833, 353, 129, 673, 961, 225, 513, 33, 705, 609, 897, 417, 321, 993, 385, 801, 65, 481, 257, 929, 577, 97, 769, 289, 193, 865, 641, 161, 449 and 737 are set at the address table memories MT(1) - MT(32), respectively, as shown in Figure 12.

The results of actual operation of display apparatus according to the above first and second embodiments are summarized in the following Table 1 together with those of the 2-interlaced scanning scheme and the 8-interlaced scanning scheme also described above.

Table 1

	2-interlaced	8-interlaced	First and second embodiment
Flicker due to scanning drive	none	none	none
Flicker due to repetition of black and white	observed	none	none
Observability of motion picture	good	poor	good

Similarly, the results of actual operation of display apparatus according to the above third and fourth embodiments are summarized in the following Table 2 together with those of the 4-interlaced scanning scheme and the 16-interlaced scanning scheme also described above.

Table 2

	4-interlaced	16-interlaced	Third and fourth embodiment
Flicker due to scanning drive	none	none	none
Flicker due to repetition of black and white	observed	none	none
Observability of motion picture	good	poor	good

Figure 13 shows a set of drive signal waveforms used in evaluation of the above embodiments and Figure 14 is a time chart showing correlation between signal transfer and drive for driving an apparatus shown in Figure 3.

In each of the above embodiments, each block is designed to have 32 scanning electrodes. This is because patterns, such as a font, an icon and a mouse mark have a height of 32 dots or less and no flicker due to scanning drive is caused by 32 lines. If the number of scanning electrodes in one block is increased, the chance of a block boundary appearing in a display pattern such as a font is lowered, thus providing a good observability, but the liability of flicker due to scanning drive is reversely increased. If the number of scanning electrodes in one block is decreased, the chance of a block boundary appearing in a display pattern such as a font is increased. Particularly, in case where the number of scanning electrodes in one block is smaller than the number of dots in the height direction of a display pattern, such as a font, a block boundary always appears in a font display and the scanning is skipped there, so that the observability is remarkably impaired.

For the above reason, it is preferred that the number of scanning electrodes in one block is (i) not as large as to cause flicker due to scanning drive, and (ii) sufficiently large as to be equal to or larger than the number of dots in height direction of a display pattern, such as a font, an icon or a mouse mark. As far as the above conditions (i) and (ii) are satisfied, a larger number provides a better observability.

As described above, in the present invention, the scanning lines are divided into a plurality of blocks each including a plurality of adjacent scanning lines, and the blocks are sequentially selected with a spacing of at least one block between successively selected blocks while consecutively selecting the adjacent scanning liens within each block. As a result, the frequency of alternation of black-displaying and white-displaying data signals for displaying a repetitive image is prevented from lowering to obviate flicker while retaining good observability of a motion picture. Thus, a display apparatus showing an improved image quality is provided.

A display apparatus includes a matrix of a group of scanning lines and a group of data signal lines intersecting the scanning lines, pixels each formed at an intersection of the scanning lines and data signal lines, and a driver for supplying drive signals to the matrix so as to effect a display at the pixels. The scanning lines are divided into at least three blocks each comprising a plurality of adjacent scanning lines. The driver includes scanning means for sequentially selecting the at least three blocks so as not to select neighboring blocks consecutively and for consecutively selecting adjacent scanning lines in a selected block. As a result, flicker in a repetitive image is prevented while maintaining good observability of a motion

picture.

Claims

1. A display apparatus, comprising: a matrix of a group of scanning lines and a group of data signal lines intersecting the scanning lines, pixels each formed at an intersection of the scanning lines and data signal lines, and drive means for supplying drive signals to the matrix so as to effect a display at the pixels;
   the scanning lines being divided into at least three blocks each comprising a plurality of adjacent scanning lines,
   the drive means including scanning means for sequentially selecting said at least three blocks so as not to select neighboring blocks consecutively and for consecutively selecting adjacent scanning lines in a selected block.

2. An apparatus according to Claim 1, wherein said pixels comprise a liquid crystal.

3. An apparatus according to Claim 1, wherein said pixels comprise a ferroelectric liquid crystal.

4. An apparatus according to Claim 1, wherein said pixels comprise a liquid crystal and are each provided with a switching element.

5. An apparatus according to Claim 1, wherein each of said at least three blocks includes the same number of scanning lines.

6. An apparatus according to Claim 1, wherein said at least three blocks are selected in an irregular sequence.

7. An apparatus according to Claim 1, further comprising illumination means for illuminating the pixels.

8. An apparatus according to Claim 1, further comprising a graphic controller for controlling a display image.

9. An apparatus according to Claim 1, further comprising recording means for recording a display image.

10. A display method, comprising:
    providing a display apparatus including a matrix of a group of scanning lines and a group of data signal lines intersecting the scanning lines, pixels each formed at an intersection of the scanning lines and data signal lines, and drive means for supplying drive signals to the matrix so as to effect a display at the pixels;
    dividing the scanning lines into at least three blocks each comprising a plurality of adjacent scanning lines,
    sequentially selecting said at least three blocks so as not to select neighboring blocks consecutively, and consecutively selecting adjacent scanning lines in a selected block.

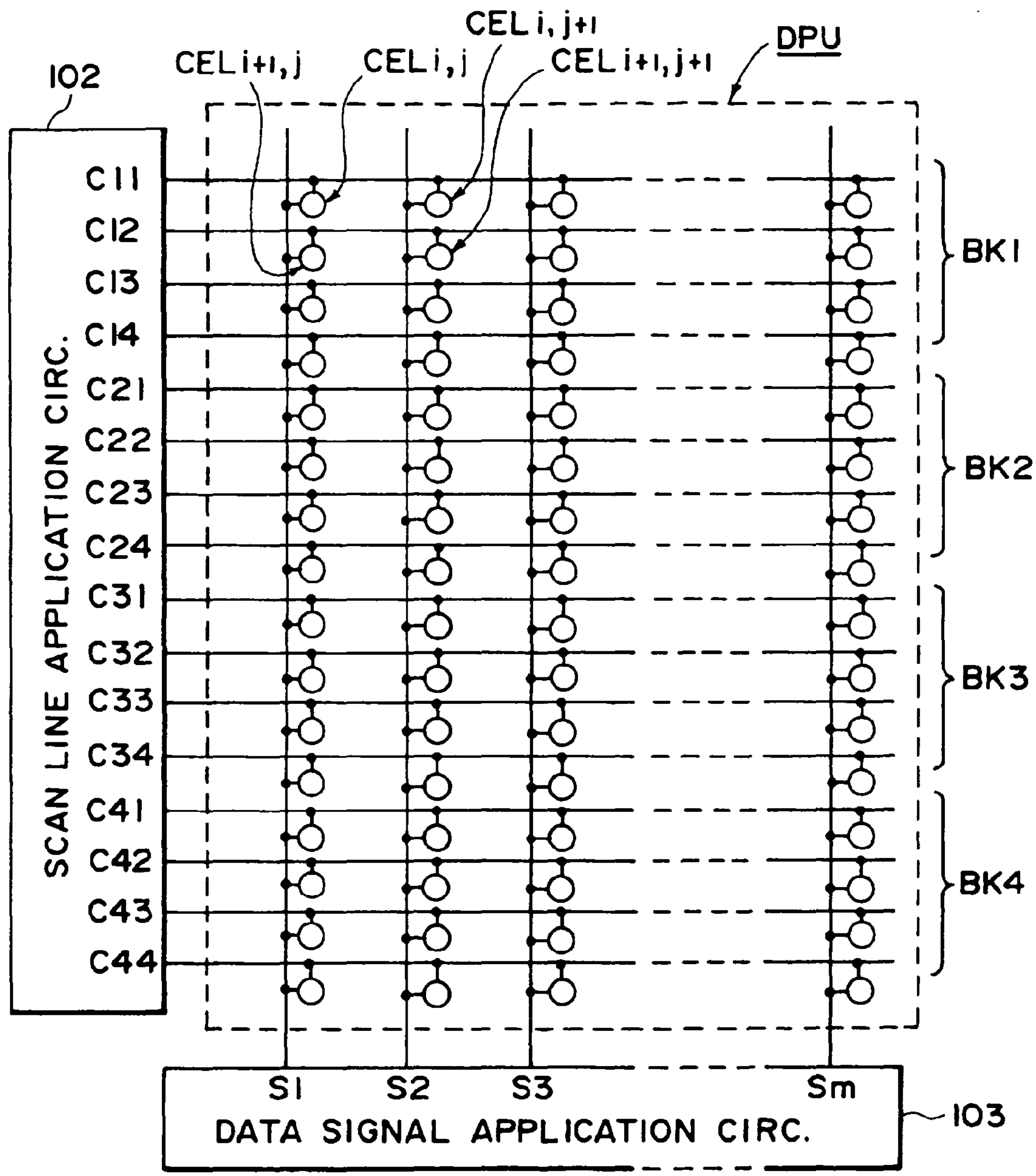
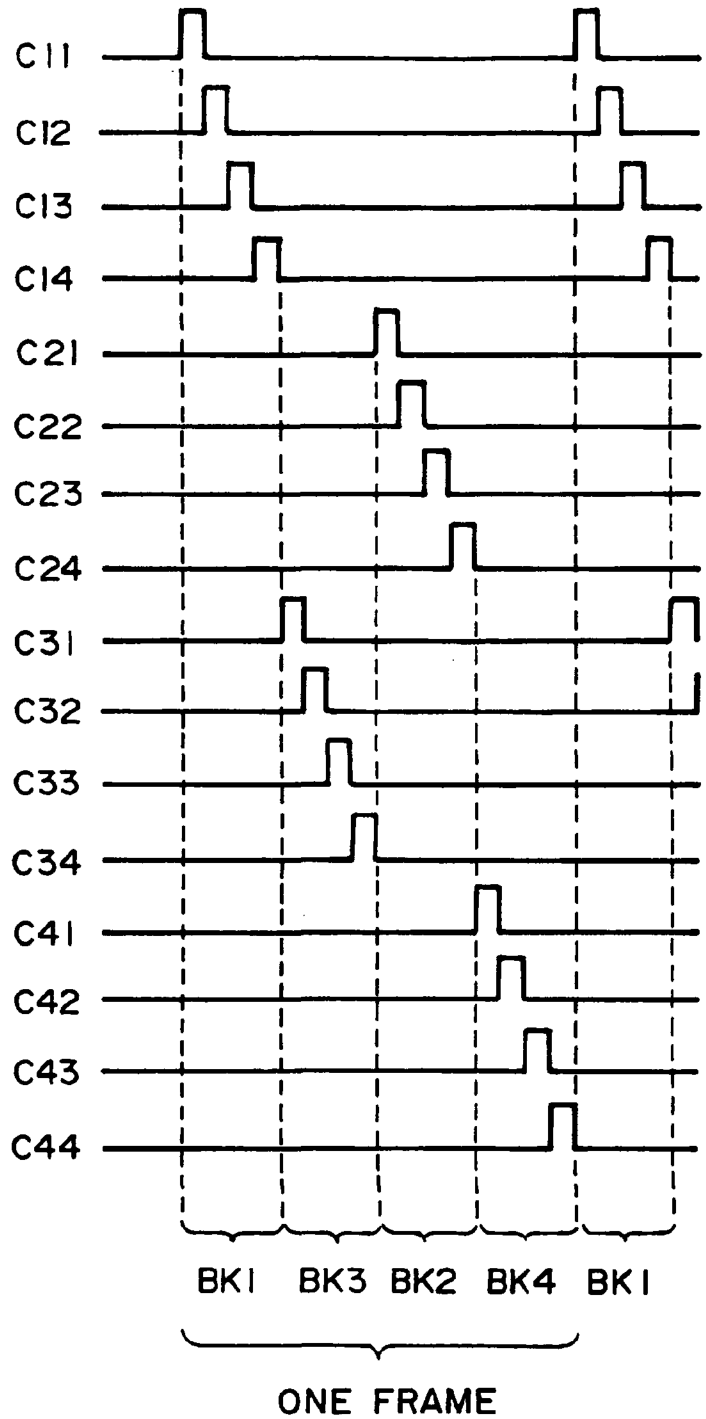

CEL i, j+1
CEL i+1, j
CEL i, j
CEL i+1, j+1
DPU
102
SCAN LINE APPLICATION CIRC.
C11
C12
C13
C14
C21
C22
C23
C24
C31
C32
C33
C34
C41
C42
C43
C44
BK1
BK2
BK3
BK4
S1
S2
S3
Sm
DATA SIGNAL APPLICATION CIRC.
103

FIG. 1


C11
C12
C13
C14
C21
C22
C23
C24
C31
C32
C33
C34
C41
C42
C43
C44
BK1
BK3
BK2
BK4
BK1
ONE FRAME

F I G. 2

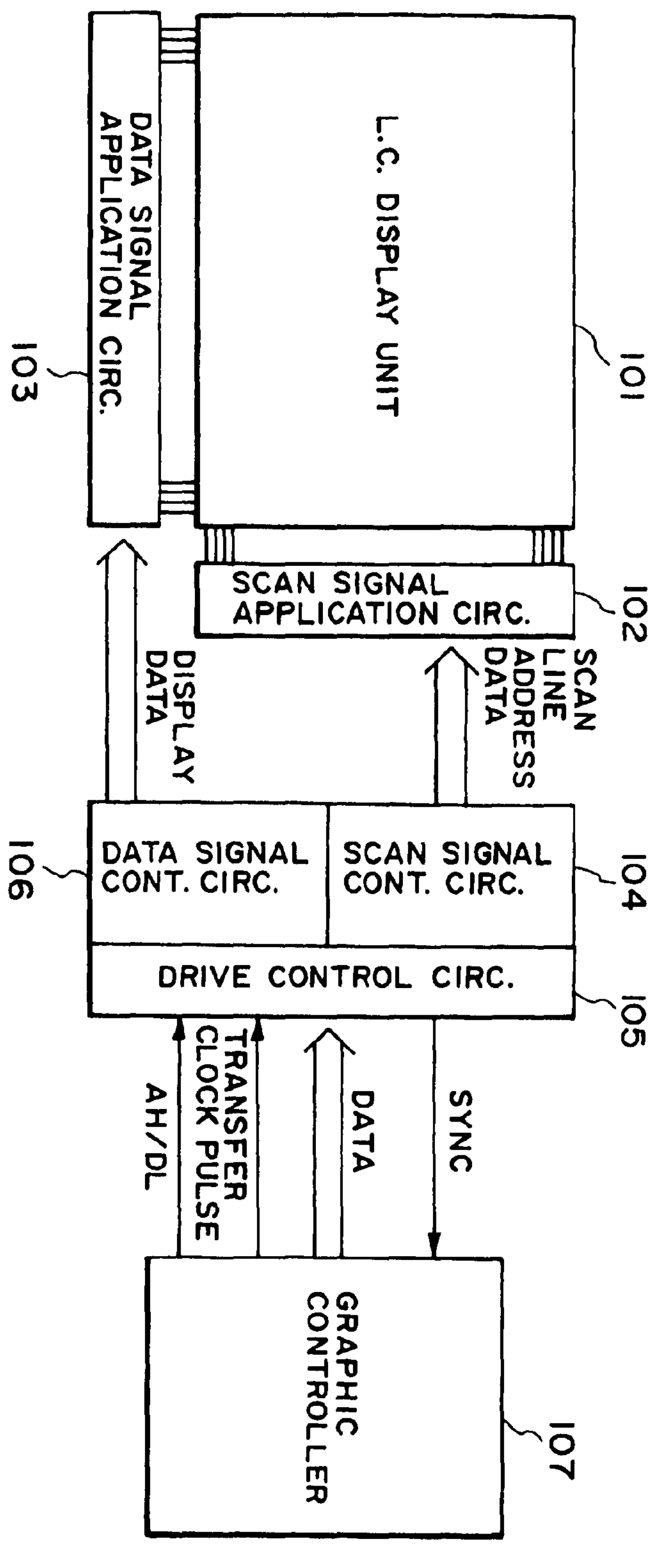

DATA SIGNAL APPLICATION CIRC.
103
L.C. DISPLAY UNIT
101
SCAN SIGNAL APPLICATION CIRC.
102
DISPLAY DATA
SCAN LINE ADDRESS DATA
DATA SIGNAL CONT. CIRC.
106
SCAN SIGNAL CONT. CIRC.
104
DRIVE CONTROL CIRC.
105
AH/DL
TRANSFER CLOCK PULSE
DATA
SYNC
GRAPHIC CONTROLLER
107

FIG. 3

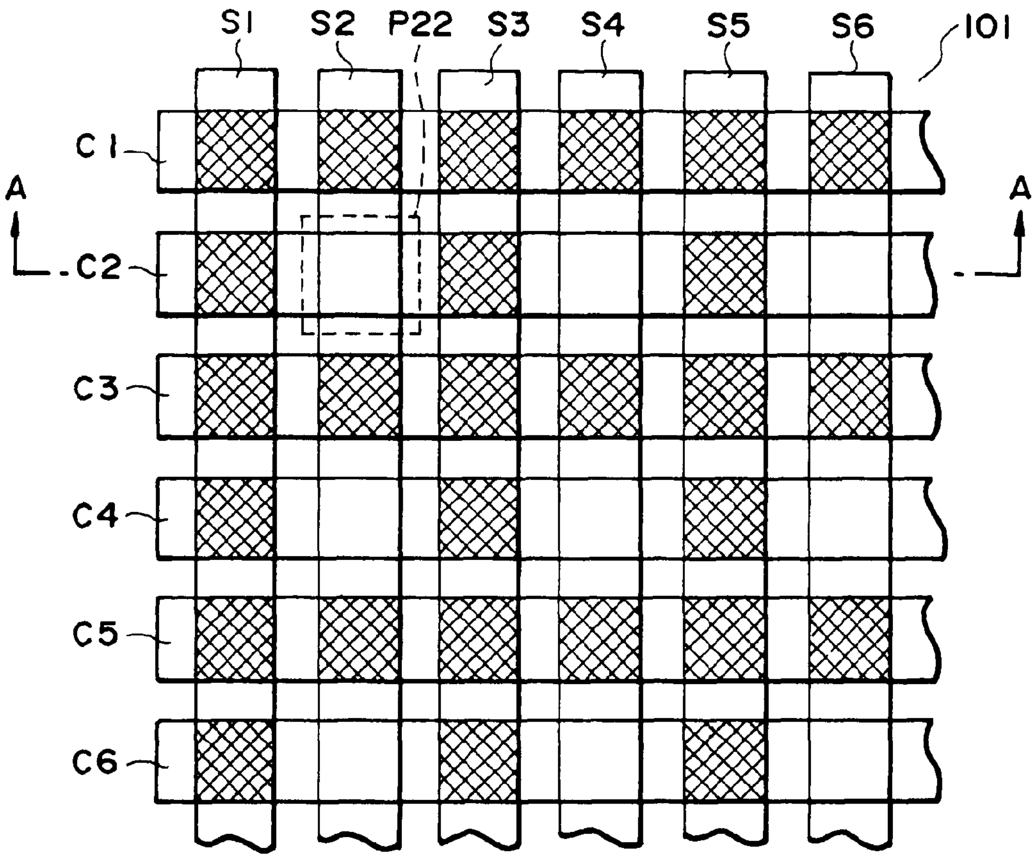

S1
S2
P22
S3
S4
S5
S6
101
C1
C2
C3
C4
C5
C6
A
A

FIG. 4

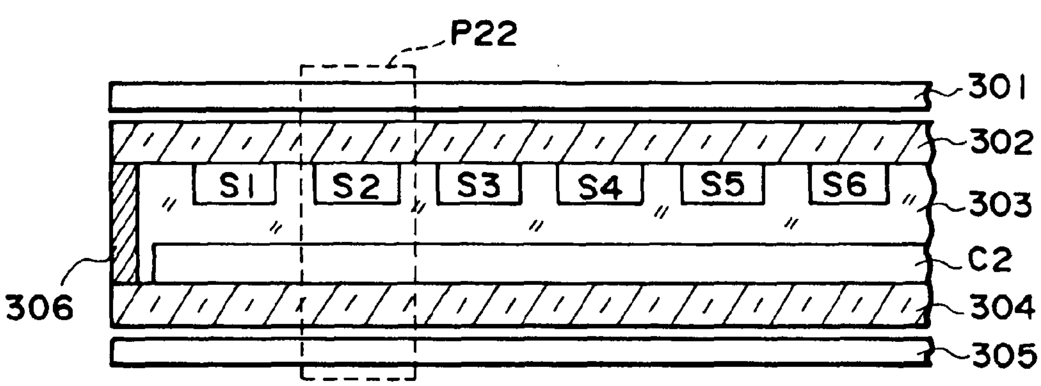

P22
301
302
S1
S2
S3
S4
S5
S6
303
C2
306
304
305

FIG. 5

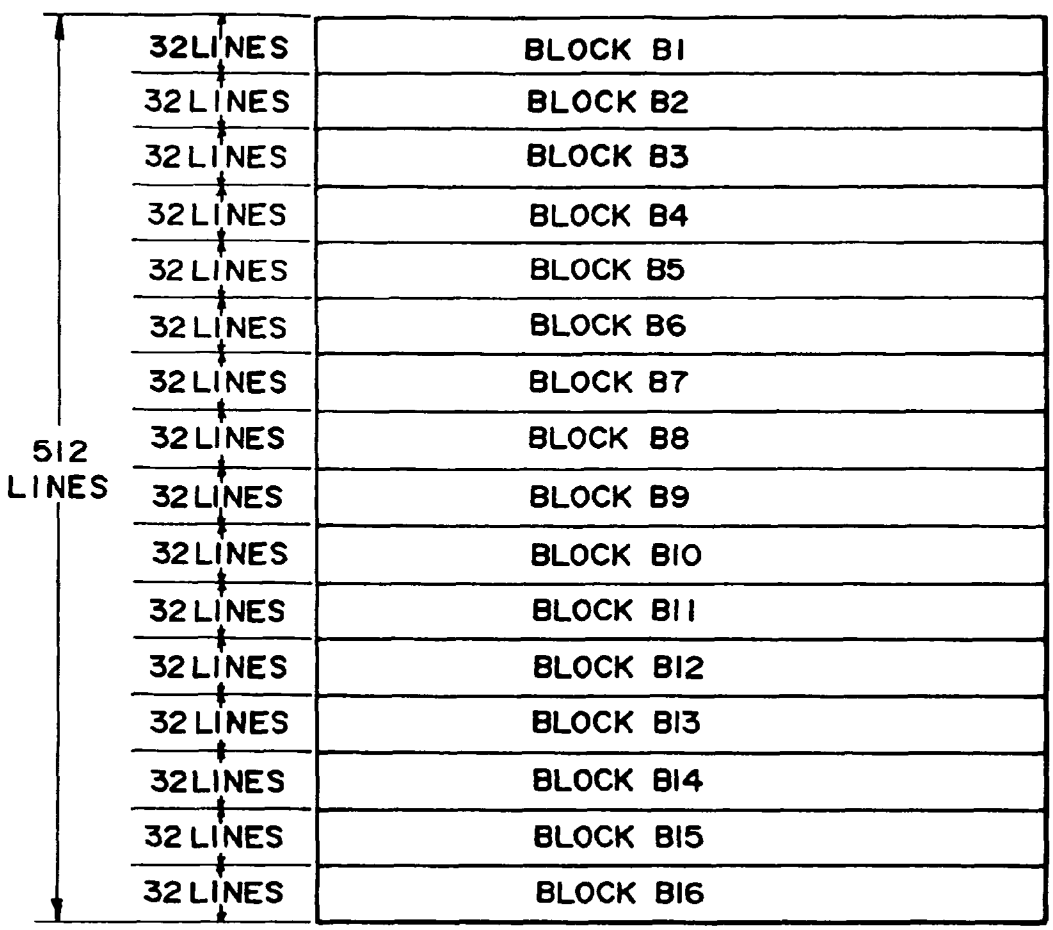

512 LINES
32 LINES
BLOCK B1
BLOCK B2
BLOCK B3
BLOCK B4
BLOCK B5
BLOCK B6
BLOCK B7
BLOCK B8
BLOCK B9
BLOCK B10
BLOCK B11
BLOCK B12
BLOCK B13
BLOCK B14
BLOCK B15
BLOCK B16

FIG. 6

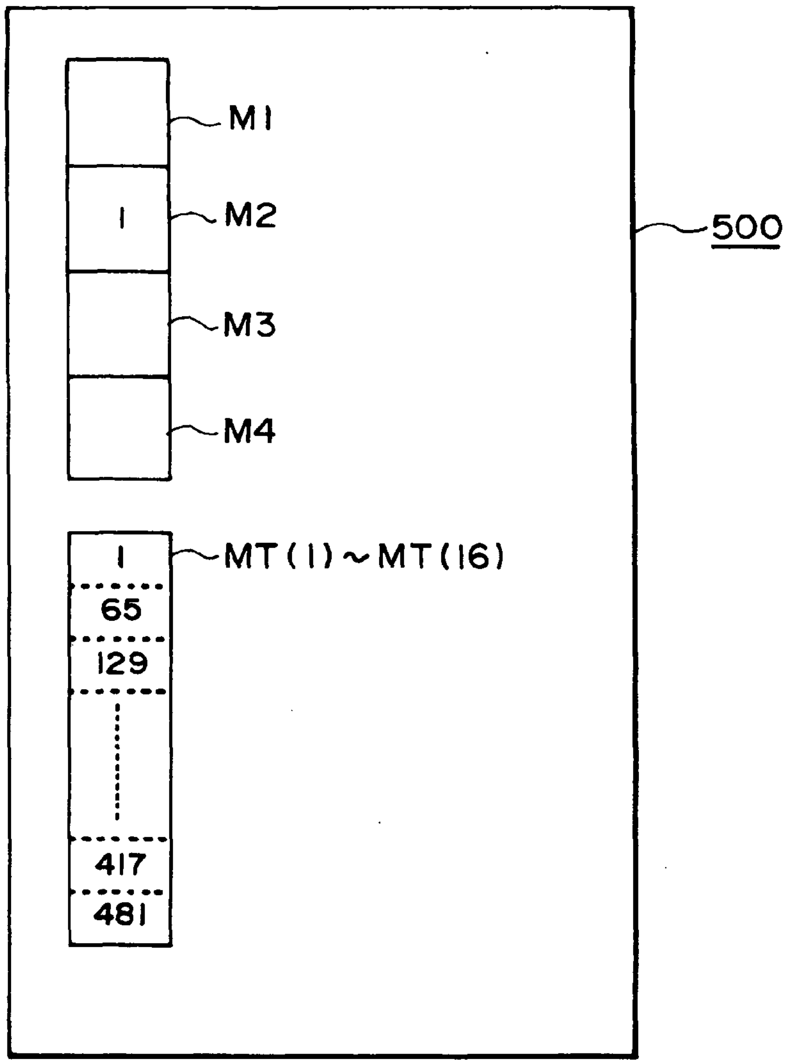
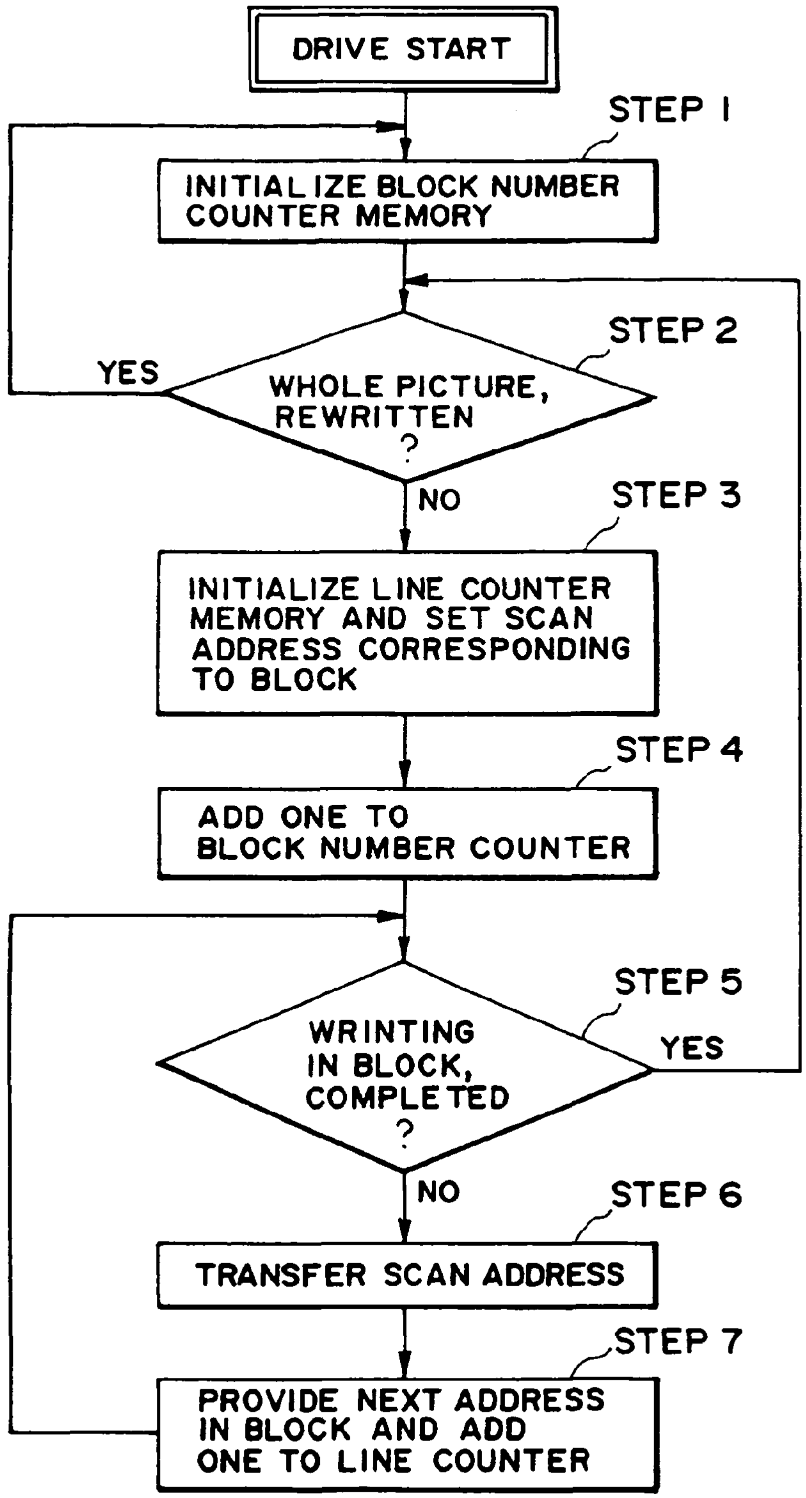
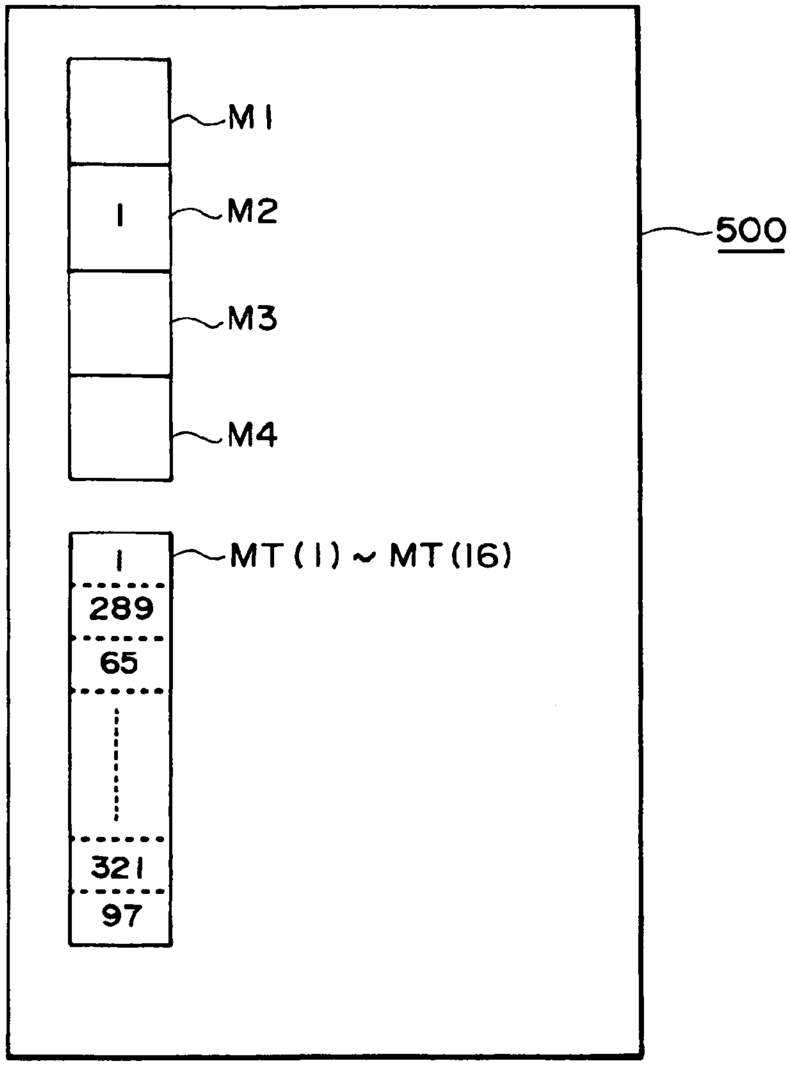


FIG. 7


DRIVE START
STEP 1
INITIALIZE BLOCK NUMBER COUNTER MEMORY
STEP 2
YES
WHOLE PICTURE, REWRITTEN ?
NO
STEP 3
INITIALIZE LINE COUNTER MEMORY AND SET SCAN ADDRESS CORRESPONDING TO BLOCK
STEP 4
ADD ONE TO BLOCK NUMBER COUNTER
STEP 5
WRINTING IN BLOCK, COMPLETED ?
YES
NO
STEP 6
TRANSFER SCAN ADDRESS
STEP 7
PROVIDE NEXT ADDRESS IN BLOCK AND ADD ONE TO LINE COUNTER

F I G. 8



F I G. 9

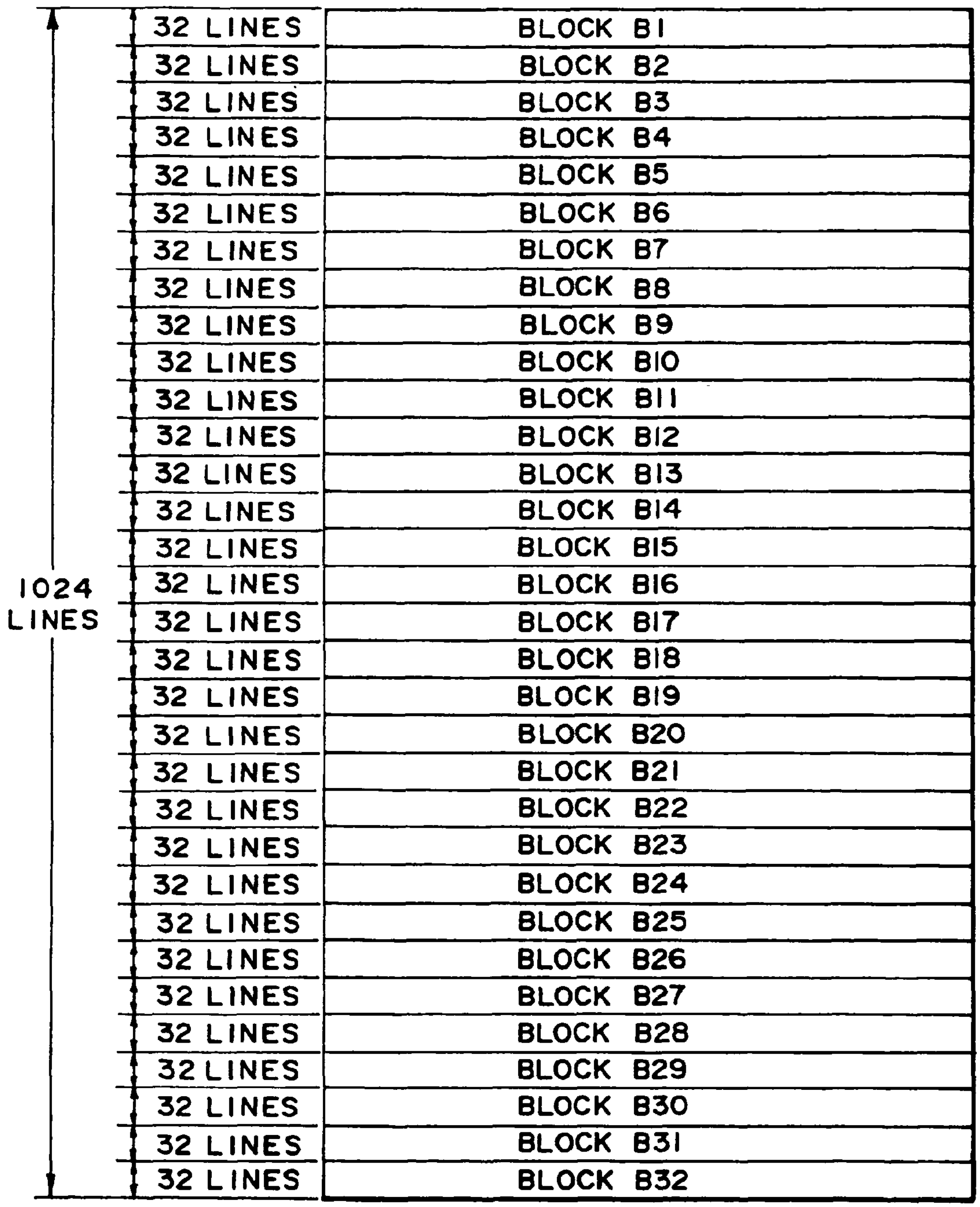

1024 LINES
32 LINES
BLOCK B1
BLOCK B2
BLOCK B3
BLOCK B4
BLOCK B5
BLOCK B6
BLOCK B7
BLOCK B8
BLOCK B9
BLOCK B10
BLOCK B11
BLOCK B12
BLOCK B13
BLOCK B14
BLOCK B15
BLOCK B16
BLOCK B17
BLOCK B18
BLOCK B19
BLOCK B20
BLOCK B21
BLOCK B22
BLOCK B23
BLOCK B24
BLOCK B25
BLOCK B26
BLOCK B27
BLOCK B28
BLOCK B29
BLOCK B30
BLOCK B31
BLOCK B32

FIG. 10

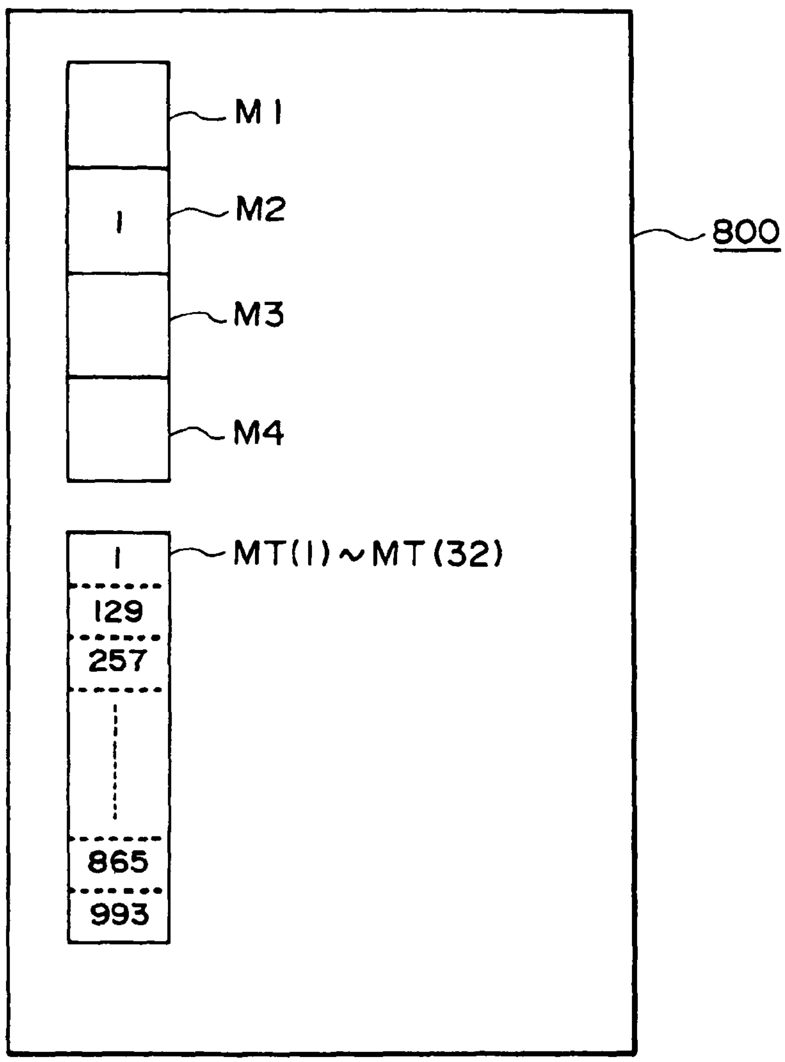


FIG. 11

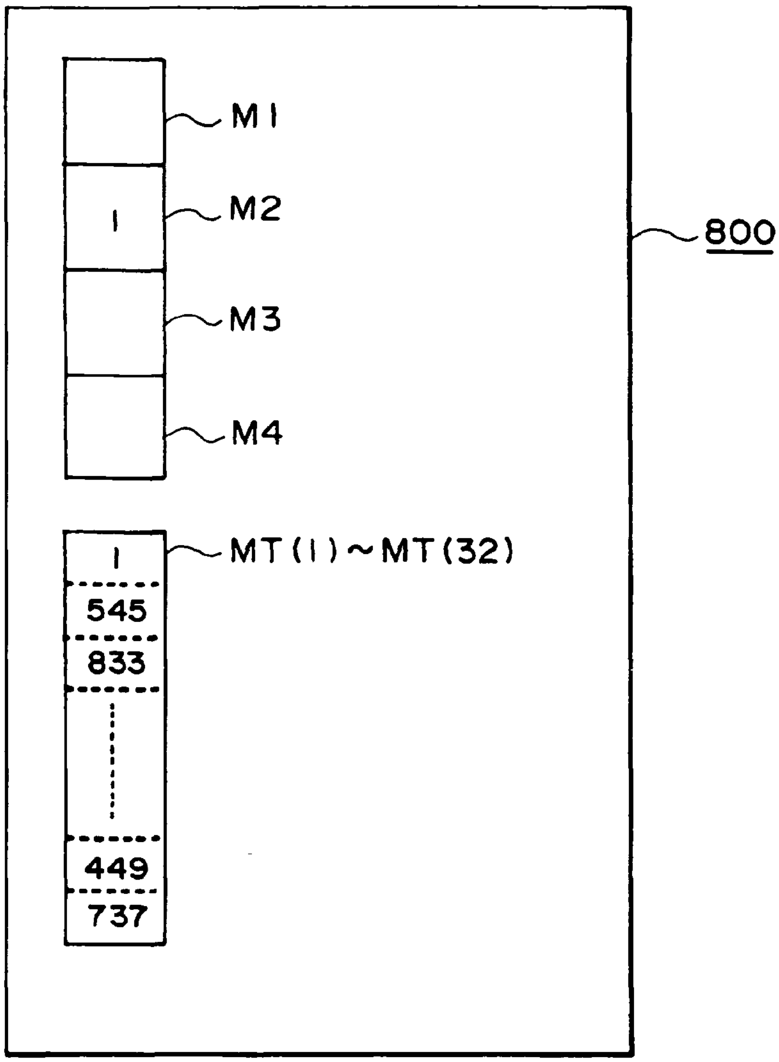


FIG. 12

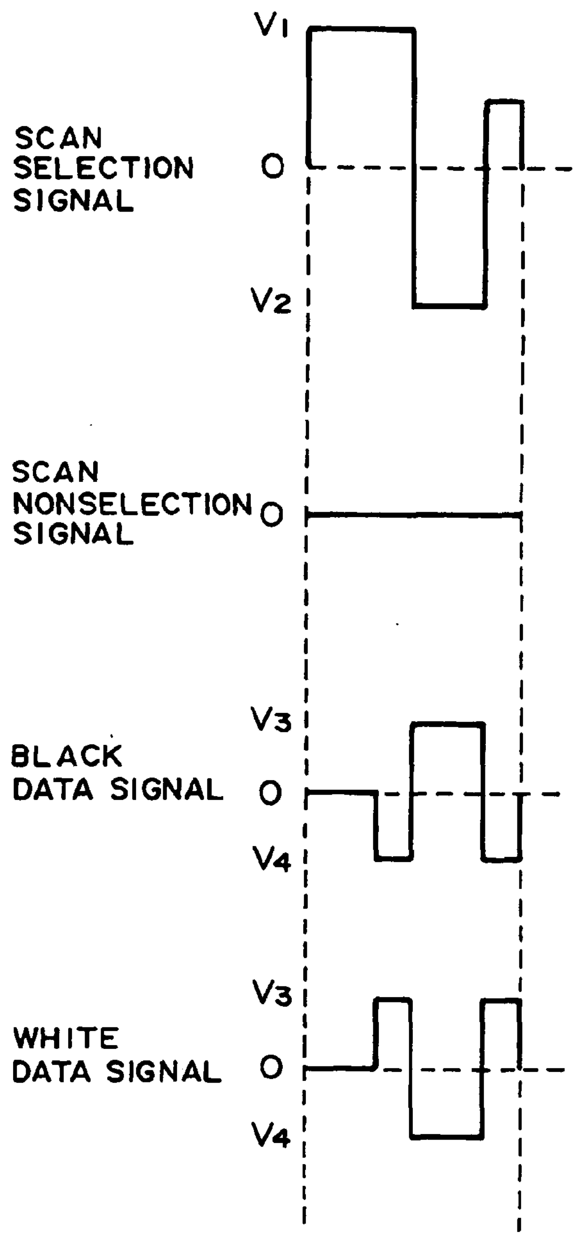

V1
SCAN
SELECTION
SIGNAL
0
V2
SCAN
NONSELECTION
SIGNAL
0
V3
BLACK
DATA SIGNAL
0
V4
V3
WHITE
DATA SIGNAL
0
V4

FIG. 13

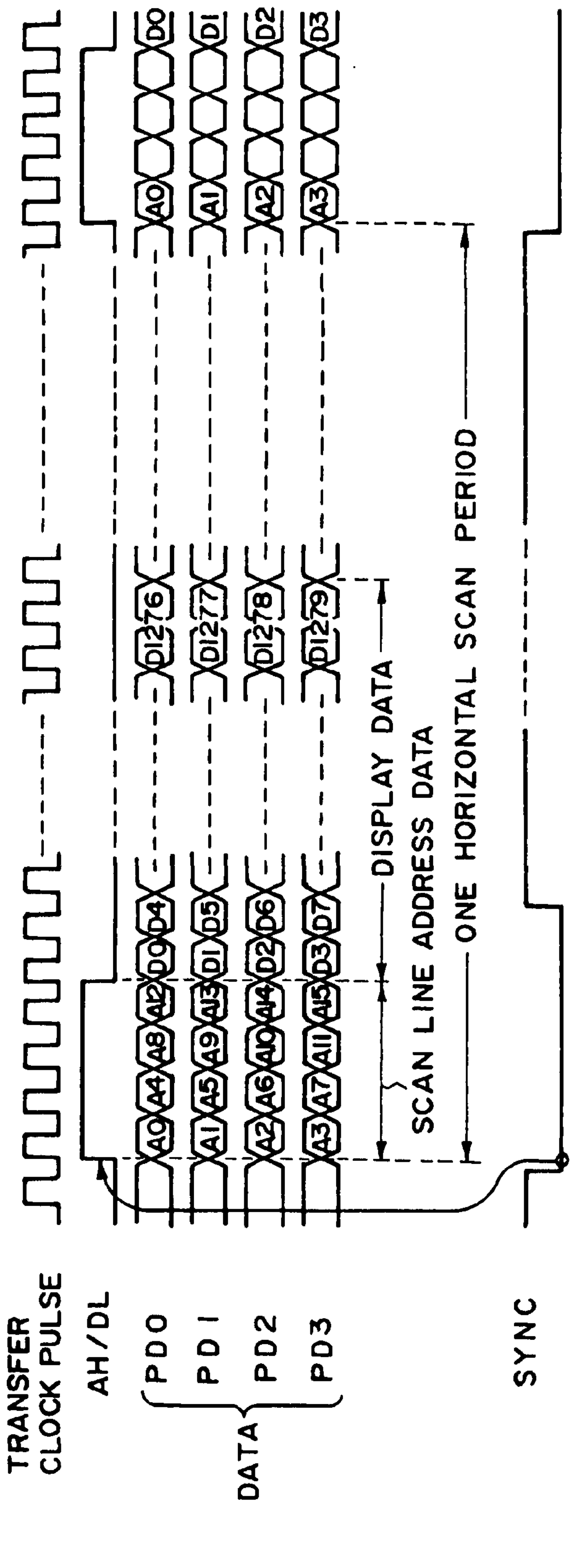

TRANSFER
CLOCK PULSE
AH/DL
DATA
PD0
PD1
PD2
PD3
SYNC
DISPLAY DATA
SCAN LINE ADDRESS DATA
ONE HORIZONTAL SCAN PERIOD

FIG. 14

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 93109196.1

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP - A - 0 434 042 (CANON) * Abstract *	1-3,5, 7,8,10	G 09 G 3/36 G 02 F 1/133
X	EP - A - 0 342 835 (STC PLC) * Abstract *	1-3,5, 7,8,10	
X	DE - C - 3 613 446 (CANON) * Abstract *	1-3,5, 7,8,10	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 02 F 1/00
G 02 G 3/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	24-09-1993	KUNZE

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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& : member of the same patent family, corresponding document